IN THE CLAIMS:

Claim 1 (Currently Amended): A semiconductor integrated circuit device comprising:

at least two ~~a plurality of~~ internal circuits arranged internally in a circuit forming region, each of said two internal circuits having a different pair of power lines;

a plurality of external signal input/output circuits having input protection circuits connected to input/output terminals outside said two internal circuits;

an inter-circuit signal wire, different from said power lines, arranged to interconnect said two internal circuits, wherein said inter-circuit signal wire is not directly connected to said external signal input/output circuits;

a first transistor forming an input element, ~~an active element in a first connection configuration~~ connected to said inter-circuit signal wire, in one of said two internal circuits; and

a plurality of second transistors, ~~other active elements in a second connection configuration~~ for protecting said first transistor, being arranged adjacent to said first transistor in said one of said two internal circuits and ~~active element in the first connection configuration~~ including ~~elements~~ a transistor of an identical structure to said ~~active element in the first connection configuration~~ first transistor,

~~said plurality of active elements in the second connection configuration being arranged adjacent to said active element in the first connection configuration to sandwich or surround said active element in the first connection configuration,~~

wherein gates of said plurality of second transistors ~~active elements in the second connection configuration being~~ are connected only to said power lines of said one of said two internal circuits ~~associated therewith~~.

Claim 2 (Currently Amended): A semiconductor integrated circuit device according to claim 1, wherein each of said internal circuits includes a plurality of basic cells regularly arranged in repetition, and said first transistor and said plurality of second transistors ~~active element in the first connection configuration and said plurality of active elements in the second connection configuration~~ are allocated to some of said basic cells.

Claim 3. (Original): A semiconductor integrated circuit device according to claim 1, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claims 4 and 5 (Canceled).

Claim 6 (Currently Amended): A semiconductor integrated circuit device according to claim [[5]] 1, wherein a plurality of said second transistors ~~active elements in the second connection configuration are~~ arranged to sandwich or surround said ~~active element in the first connection configuration~~ first transistor.

Claim 7 (Currently Amended): A semiconductor integrated circuit device according to claim [[5]] 6, wherein each of said internal circuits includes a plurality of basic cells regularly arranged in repetition, and said first transistor and said plurality of transistors ~~active element in the first connection configuration and said plurality of active elements in the second connection configuration~~ are allocated to some of said basic cells.

Claim 8 (Currently Amended): A semiconductor integrated circuit device according to claim [[5]] 6, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claims 9-11 (Canceled).

Claim 12 (Withdrawn): A semiconductor integrated circuit device according to claim 10, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the second connection configuration, and said active elements in the third connection configuration are allocated to some of said basic cells.

Claim 13 (Withdrawn): A semiconductor integrated circuit device according to claim 10, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claim 14 (Withdrawn): A semiconductor integrated circuit device according to claim 13, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

Claims 15 and 16 (Canceled).

Claim 17 (Withdrawn): A semiconductor integrated circuit device according to claim 15, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the second connection configuration, and said active elements in the third connection configuration are allocated to some of said basic cells.

Claim 18 (Withdrawn): A semiconductor integrated circuit device according to claim 15, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claim 19 (Withdrawn): A semiconductor integrated circuit device according to claim 18, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

Claim 20 (Withdrawn): A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having difference power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits; and

an inter-circuit auxiliary wire connected to a static area near a location at which said inter-circuit signal wire is connected.

Claim 21 (Withdrawn): A semiconductor integrated circuit device according to claim 20, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition.

Claim 22 (Withdrawn): A semiconductor integrated circuit device according to claim 20, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claim 23 (Withdrawn): A semiconductor integrated circuit device according to claim 22, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

Claim 24 (Withdrawn): A semiconductor integrated circuit device according to claim 20, wherein said static area includes a partial region of an active element on a transmission side of said active elements in the first connection configuration connected to said inter-circuit signal wire, said partial region being connected to a power line of said internal circuit associated therewith, and an active element in another connection configuration having an identical or similar structure to said active element in the first connection configuration on a reception side, and arranged near said active element in the first connection configuration, said active element in the other connection configuration being isolated from signal wires other than said inter-circuit auxiliary wire.

Claim 25 (Withdrawn): A semiconductor integrated circuit device according to claim 24, wherein a plurality of said active elements in the other connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

Claim 26 (Withdrawn): A semiconductor integrated circuit device according to claim 24, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration and said active elements in the other connection configuration are allocated to some of said basic cells.

Claim 27 (Withdrawn): A semiconductor integrated circuit device according to claim 24, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claim 28 (Withdrawn): A semiconductor integrated circuit device according to claim 27, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

Claim 29 (Withdrawn): A semiconductor integrated circuit device according to claim 24, wherein said inter-circuit auxiliary wire is connected to a neighboring region overlapping with or close to said partial region on said power line connected thereto, instead of said partial region.

Claim 30 (Withdrawn): A semiconductor integrated circuit device according to claim 24, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged in any pair of said plurality of internal circuits;

an active element in a further connection configuration having an identical or similar structure to said active element in the other connection configuration is arranged in addition to said active element in the other connection configuration near an active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits, said active element in the

further connection configuration being connected to a power line of said internal circuit and being isolated from said inter-circuit signal wire, other signal wires and said inter-circuit auxiliary wire; and

said active elements in the other connection configuration are arranged instead of or exclusive of said active element in the further connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other of said pair of internal circuits.

Claim 31 (Withdrawn): A semiconductor integrated circuit device according to claim 30, wherein a group of elements including a plurality of either said active elements in the first connection configuration, said active elements in the other connection configuration, or said active elements in the further connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

Claim 32 (Withdrawn): A semiconductor integrated circuit device according to claim 30, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the other connection configuration, and said active elements in the further connection configuration are allocated to some of said basic cells.

Claim 33 (Withdrawn): A semiconductor integrated circuit device according to claim 30, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claim 34 (Withdrawn): A semiconductor integrated circuit device according to claim 33, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

Claim 35 (Withdrawn): A semiconductor integrated circuit device according to claim 29, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged in any pair of said plurality of internal circuits;

an active element in a further connection configuration having an identical or similar structure to said active element in the other connection configuration is arranged in addition to said active element in the other connection configuration near an active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits, said active element in the further connection configuration being connected to a power line of said internal circuit and being isolated from said inter-circuit signal wire, other signal wires and said inter-circuit auxiliary wire; and

said active elements in the other connection configuration are arranged instead of or exclusive of said active element in the further connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other of said pair of internal circuits.

Claim 36 (Withdrawn): A semiconductor integrated circuit device according to claim 35, wherein a group of elements including a plurality of either of said active elements in the first connection configuration, said active elements in the other connection configuration, or said active elements in the further connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

Claim 37 (Withdrawn): A semiconductor integrated circuit device according to claim 35, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the other connection configuration, and said active elements in the further connection configuration are allocated to some of said basic cells.

Claim 38 (Withdrawn): A semiconductor integrated circuit device according to claim 35, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claim 39 (Withdrawn): A semiconductor integrated circuit device according to claim 38, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

Claim 40 (Withdrawn): A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having difference power lines;

a plurality of input/output circuits arranged outside said internal circuits;

a plurality of external connection terminals outside said input/output circuits;

a signal wire passing through an input/output circuit in one of a plurality of sets comprised of any of said internal circuits and any of said input/output circuit, said plurality of sets being connected to common power lines, said signal wire reaching said internal circuit included in the same set as said input/output circuit from any of said external connection terminals;

a branched wire branched from said signal wire and passing through said input/output circuit in any other set of said plurality of sets, and reaching said internal circuit in the same set as said input/output circuit;

a first protection circuit arranged in said input/output circuit of said one set for said signal wire;

a second protection circuit arranged in said input/output circuit in another set for said branched wire; and

a third protection circuit arranged in said internal circuit in said other set for said branched wire.

Claim 41 (Withdrawn): A semiconductor integrated circuit device according to claim 40, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition.

Claim 42 (Withdrawn): A semiconductor integrated circuit device according to claim 40, further comprising substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Claim 43 (Withdrawn): A semiconductor integrated circuit device according to claim 40, wherein said third protection circuit includes a plurality of protection elements, said protection elements being arranged to sandwich or surround an element to be protected.

Claim 44 (Withdrawn): A semiconductor integrated circuit device according to claim 40, wherein either of said first, second or third protection circuit includes an active element connected to a power line of an associated input/output circuit or an associated internal circuit, and isolated from any signal wire.

Claim 45 (Withdrawn): A semiconductor integrated circuit device according to claim 44, wherein said third protection circuit includes a plurality of protection elements, said protection elements being arranged to sandwich or surround an element to be protected.

Claim 46 (NEW): A semiconductor integrated circuit device according to claim 1, wherein said first transistor is an n-type MOS transistor and said transistor of an identical structure to said first transistor is an n-type MOS transistor.

Claim 47 (NEW): A semiconductor integrated circuit device according to claim 46, wherein a drain of said transistor of an identical structure to said first transistor is connected to one of said power lines of said one of said two internal circuits.

Claim 48 (NEW): A semiconductor integrated circuit device according to claim 46, wherein a drain of said transistor of an identical structure to said first transistor is connected to said inter-circuit signal wire.

Claim 49 (NEW): A semiconductor integrated circuit device according to claim 1, wherein said first transistor is a p-type MOS transistor and said transistor of an identical structure to said first transistor is a p-type MOS transistor.